IN THE SPECIFICATION

Please **amend** the section title on line 3 of page 1 of the specification as follows.

~~BACKGROUND OF THE INVENTION~~ CROSS-REFERENCES TO RELATED APPLICATIONS

Please **insert** the following section title on line 6 of page 1 of the specification.

BACKGROUND OF THE INVENTION

Please **replace** the paragraph beginning on line 1 of page 8 of the specification with the following re-written paragraph.

Figure 2 is a block diagram of a multi-pass demodulation receiver 300. Multi-pass demodulation receiver 300 comprises a demodulator 302, de-interleaver 304, channel decoder 306, and re-encoder 308. The received signal is converted to the baseband frequency and input to demodulator ~~203~~ 302. During the first pass through the demodulator 302, the received signal is demodulated in a conventional fashion. The received sequence output from demodulator 302 is fed to de-interleaver 304, which reorders the bits of the received sequence. The output from de-interleaver 304 is fed to channel decoder 306, which detects and corrects errors that may have occurred during transmission. The output from channel decoder 306 is an estimate of the original information sequence transmitted from the transmitter 100. The output from channel decoder 306 is then re-encoded in re-encoder 308 and selected ones of the re-encoded bits are fed back to the demodulator 302 to use as pilot bits in second pass demodulation. During second pass demodulation, the re-encoded bits fed back from channel decoder 306 are treated as known bits by the demodulator 302. Thus, during second pass demodulation, the demodulator 302 is constrained to output symbols that meet the known bit pattern. The re-encoded bits output by channel decoder 306 may be "hard bits" or may be "soft

bits" reflecting the level of confidence in the decision. In either case, well-known methods exist for exploiting the decisions in the demodulator 302.